AMENDMENTS TO THE DRAWINGS

Replacement formal drawings of Figures 1-7 are submitted concurrently herewith under a separate cover letter.

REMARKS

By this Amendment, claim 1 is amended. Thus, claim 1 is active in the application. Reexamination and reconsideration of the application are respectfully requested.

The specification and abstract have been carefully reviewed and revised in order to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. No new matter has been added.

Also attached hereto is a marked-up version of the substitute specification and abstract illustrating the changes made to the original specification and abstract.

In item 1 on page 2 of the Office Action, the Examiner required that Figures 5-7 be labeled as "Prior Art." Pursuant to this requirement, Figures 5-7 have been labeled as "Prior Art."

In item 2 on page 2 of the Office Action, the Examiner objected to the drawings for not illustrating that (1) a periphery of an upper dielectric layer of the first dielectric layer is positioned identically in size and shape to a periphery of a lower dielectric layer of the first dielectric layer, and (2) a periphery of an upper dielectric layer of the second dielectric layer is positioned identically in size and shape to a periphery of a lower dielectric layer of the second dielectric layer, as recited in original claim 1.

This feature of the present invention has been cancelled from claim 1. Accordingly, the drawings have not been revised to illustrate this feature. However, Figure 4, which is a sectional view of Figure 3, has been revised to illustrate the periphery of the upper dielectric layer 7b of the first dielectric layer 7 and the periphery of the lower dielectric layer 7a of the first dielectric layer 7. In particular, reference numeral 21 has been added to Figure 4 to denote the periphery of the upper dielectric layer 7b, and reference numeral 22 has been added to illustrate the periphery of the lower dielectric layer 7a. As mentioned above, Figure 4 is a sectional view of Figure 3, and these features of the present invention are also illustrated in Figure 3. Accordingly, no new matter has been added via the revisions to Figure 4.

Replacement formal drawings of Figures 1-7 containing the aforementioned revisions to the drawings are submitted concurrently herewith under a separate cover letter. Approval of the replacement formal drawings is respectfully requested.

In item 4 on page 4 of the Office Action, claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Nishiki et al. (U.S. 6,261,144). Furthermore, in item 6 on page 5 of the Office Action, claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hiroyuki et al. (JP 09-259768).

Without intending to acquiesce to these rejections, claim 1 has been amended to more clearly illustrate the marked differences between the present invention and the applied references. Accordingly, the Applicant respectfully submits that the present invention is clearly patentable over the applied references for the following reasons.

The present invention, as recited in claim 1, provides a plasma display panel comprising a front substrate, a back substrate, a display electrode provided on the front substrate and formed of a scanning electrode and a sustain electrode, and a data electrode provided on the back substrate. The plasma display panel of claim 1 also comprises a multilayered first dielectric layer for covering the display electrode, and a multilayered second dielectric layer for covering the data electrode. Furthermore, the plasma display panel of claim 1 comprises a sealing member for sealing the plasma display panel, where the sealing member intervenes between the front substrate and the back substrate arranged so as to face each other.

Claim 1 defines that at least one of a periphery of an upper dielectric layer of the first dielectric layer is positioned partially in size and shape to a periphery of a lower dielectric layer of the first dielectric layer, and a periphery of an upper dielectric layer of the second dielectric layer is positioned partially in size and shape to a periphery of a lower dielectric layer of the second dielectric layer. Furthermore, claim 1 defines that the periphery of the first dielectric layer is covered with the sealing member.

As described lines 13-20 on page 10 of the substitute specification (lines 3-9 on page 10 of the original specification), the above-described structure of the plasma display panel of the present invention provides the plasma display panel with dielectric layers having excellent characteristics of breakdown voltage, and prevents bubbles from being generated on the periphery of the dielectric layers.

Nishiki et al. discloses a plasma display panel in which the dielectric layers 17-18 of the front substrate 14 and the dielectric layers 12-13 of the back substrate 10 use SiO_2 instead of a low melting-point glass. Nishiki et al. discloses that the thick film upper dielectric layer 18 is provided on the lower dielectric layer 17 of the front substrate 14 and that the thick film upper dielectric layer 13 is provided on the lower dielectric layer 12 of the back substrate 10 in order to avoid the generation of open circuits of electrode lines (see Column 9, line 39 to Column 10, line 43 and Figures 7A-7B). Nishiki et al. also discloses that a sealing member 20 seals the front substrate 14 and the back substrate 10.

However, Nishiki et al. does not disclose or suggest that the periphery of the multilayered first dielectric layer, including the lower dielectric layer 17 and the thick film upper dielectric layer 18, provided on the front substrate 14 is covered by the sealing member 20. Instead, Nishiki et al. discloses in Figures 7A-7B that the thick film upper dielectric layer 18 does not even cover the periphery of the lower dielectric layer 17 of the front substrate, and that the sealing member 20 merely extends between the thick film upper dielectric layer 18, 13 of the front and back substrates 14, 10. Accordingly, Nishiki et al. clearly does not disclose or suggest that the sealing member 20 covers the periphery of the multilayered first dielectric layer 17, 18 provided on the front substrate 14.

Therefore, Nishiki et al. clearly does not disclose or suggest a sealing member for sealing the plasma display panel, where the periphery of the first dielectric layer is covered with the sealing member, as recited in claim 1.

Accordingly, claim 1 is clearly not anticipated by Nishiki et al. since Nishiki et al. fails to disclose each and every limitation of claim 1.

Hiroyuki et al. discloses a plasma display panel in which a dielectric layer 17 of a front substrate 11 is a double layer and a dielectric layer 24 of a back substrate 21 is a single layer in order to make an addressing voltage lower and to facilitate driving of the panel.

However, similar to Nishiki et al., Hiroyuki et al. does not disclose that a periphery of a lower dielectric layer of the dielectric layer 17 provided on the front substrate 11 is covered by a sealing member for sealing the plasma display panel.

Therefore, Hiroyuki et al. also does not disclose or suggest a sealing member for

sealing the plasma display panel, where the periphery of the multilayered first dielectric layer is covered with the sealing member, as recited in claim 1.

Accordingly, Hiroyuki et al. clearly does not disclose or suggest each and every limitation of claim 1, and therefore, no obvious modification of Hiroyuki et al. would result in the invention of claim 1.

Furthermore, no obvious combination of Nishiki et al. and Hiroyuki et al. would result in the invention of claim 1 since both Nishiki et al. and Hiroyuki et al. clearly fail to disclose or suggest that the periphery of the multilayered first dielectric layer provided on the front substrate is covered with a sealing member, as recited in claim 1.

Moreover, Nishiki et al. and Hiroyuki et al. do not disclose, suggest or contemplate an effect of providing the plasma display panel with dielectric layers having excellent characteristics of breakdown voltage and preventing bubbles from being generated on the periphery of the dielectric layers, as accomplished by the plasma display panel of claim 1.

Therefore, the Applicant respectfully submits that a person having ordinary skill in the art at the time the invention was made would not have been motivated to modify Nishiki et al. and Hiroyuki et al. in such as manner as to result in, or otherwise render obvious, the present invention as recited in claim 1.

Therefore, it is submitted that the claim 1 is clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

Morio FUJITANI

By: _____
Jonathan R. Bowser
Registration No. 54,574
Attorney for Applicant

JRB/nrj
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
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